

Planning and Quality Assurance Affairs

Form (A)

Course Specifications

General Information

Course name	Digital Logic Design
Course number	ITCC2303
Faculty	
Department	
Course type	Major Needs
Course level	2
Credit hours (theoretical)	3
Credit hours (practical)	0
Course Prerequisites	

Course Objectives

- 1 - Introduce the Numbering systems in general and Binary Numbering systems in particular
- 2 - Principles of Digital Design, their theories and their applications
- 3 - Introduce the Boolean Algebra and gate level minimization
- 4 - Introduce Combinational Logic and designing fundamental Combinational Circuits
- 5 - Introduce Synchronous sequential Logic and designing fundamental sequential Circuits
- 6 - Introduce Registers and Counters and their design
- 7 - Introduce Memory and Programmable Logic

Intended Learning Outcomes

Knowledge and Understanding	* A1. Understand the concept of Binary systems and its application in Digital Design * A2. Understand and recognize Digital Logic Gates * A3. Understand the concepts of Combinational and sequential Circuits * A4. Understand the concept of Registers, Counters, Memory, and Programmable Logic. * A5. Identify the different Application areas of Digital Design
Intellectual Skills	* B1. Analyze Digital Circuits and their functionalities * B2. Compare and criticize different Digital Circuits * B3. Programming PROM and Logic Array
Professional Skills	* C1. Learn the essentials of the Logic Gates * C2. Building the truth tables * C3. Constructing the Boolean function * C4. Gate Level minimization * C5. Constructing the Digital Circuit
General Skill	* D1. Work in a group in order to build different Logic Circuits * D2. Deploy communication skills

Course Contents

1 - Digital systems, Binary Numbers, Number Base Conversions, Octal and Hexadecimal Numbers
2 - Signed Binary Numbers, Binary Codes, Binary Logic
3 - Axiomatic definition of Boolean Algebra, Basic Theorems and Properties of Boolean Algebra, Conical and Standard forms, Digital Logic gates
4 - The Map Method, Four Variable Map, Product of Sums simplification
5 - Dont care Conditions, NAND and NOR implementations, Exclusive OR Function
6 - Combinational Circuits, Analysis procedure, Design Procedure
7 - Binary Adder, Decimal Adder
8 - Magnitude Comparator, Decoders
9 - Encoders, Multiplexers
10 - Sequential Circuits, Latches, Flip=Flops
11 - Registers, Shift Registers
12 - Ripple Counters, Synchronous Counters, Other Counters
13 - Analysis of Clocked Sequential Circuits
14 - Random Access Memory, Read Only Memory

Teaching and Learning Methods

1 - Lectures
2 - Tutorial Exercises
3 - Project and/or Assignments

Students Assessment

<u>Assessment Method</u>	<u>TIME</u>	<u>MARKS</u>
Mid-Term Exam I	6th week	20
Practical Exam	12th week	20
Class Work	During the 16 weeks	10
Final Exam	16th week	50

Books and References

Course note	Lectures Notes
Essential books	Digital Design, 3 rd edition, M. Morris Mano, Prentice Hall, 2002
Recommended books	Introduction to Digital Logic Design, J. P. Hayes Addison Wesley, 1993

Knowledge and Skills Matrix

Main Course Contents	Study Week	Knowledge and Understanding	Intellectual Skills	Professional Skills	General Skill
Digital systems, Binary Numbers, Number Base Conversions, Octal and Hexadecimal Numbers	1	a1,a3	b1	c2	d1
Signed Binary Numbers, Binary Codes, Binary Logic	2	a2,a4	b1	c1	d1
Axiomatic definition of Boolean Algebra, Basic Theorems and Properties of Boolean Algebra, Conical and Standard forms, Digital Logic gates	3	a1,a2	b1	c1,c2	d2
The Map Method, Four Variable Map, Product of Sums simplification.	4	a4,a5	b1,b3	c3,c4,c5	d2
Dont care Conditions, NAND and NOR implementations, Exclusive OR Function.	5	a1,a2,a3	b1,b2	c1-c4	d1-d2
Combinational Circuits, Analysis procedure, Design Procedure	6	a1,a3,a5	b2	c1,c3,c5	d2
Binary Adder, Decimal Adder	7	a1,a2	b3	c4-c5	d1
Magnitude Comparator, Decoders	8	a1	b1	c4,c5	d1
Encoders, Multiplexers	9	a1	b1	c5	d2
Sequential Circuits, Latches, Flip=Flops	10	a1-a3	b1	c2-c4	d1-d2
Registers, Shift Registers	11	a1	b2	c3,c5	d2
Ripple Counters, Synchronous Counters, Other Counters	12	a1	b1	c2	d1
Analysis of Clocked Sequential Circuits	13	a3	b1	c5	d2
Random Access Memory, Read Only Memory	14-15	a4	b1	c2-c5	d1-d2